CLAIMS

What is claimed is:

1. A circuit comprising:

a first delay line having a first input terminal operable to receive a first input signal, a first reset terminal operable to receive a first reset signal, and a first output terminal operable to provide a first output signal in response to said first input signal;

a second delay line having a second input terminal operable to receive a second input signal, a second reset terminal operable to receive a second reset signal, and a second output terminal operable to provide a second output signal in response to said second input signal; and

a speed comparison logic module interconnected with said first output terminal, with said second output terminal, and with an evaluate terminal operable to receive an evaluate signal, said speed comparison logic module having at least one logic output terminal operable to assert a logic output signal in response to a comparison of said evaluate signal with one of said first output signal and said second output signal.

2. The circuit of claim 1 further comprising a voltage supply bus interconnected with voltage supply terminals of said first delay line and of said second delay line.

3. The circuit of claim 1 further comprising a test pulse generator operable to provide said first input signal and said second input signal, said test pulse generator interconnected with said first input terminal and with said second input terminal.

4. The circuit of claim 3 wherein said test pulse generator is interconnected with said first reset terminal and with said second reset terminal.

5. The circuit of claim 1 wherein said first delay line comprises a chain of inverters.

6. A method for evaluating the speed of a circuit, said method comprising:

concurrently launching a first input signal into a first delay line and applying a reset signal to a second delay line, such that all signals propagating through said second delay line are eliminated;

initiating an evaluate signal;

receiving a first output signal from said first delay line in response to said first input signal;

receiving said evaluate signal;

asserting an output logic signal dependent on the time of said receiving said first output signal relative to the time of said receiving said evaluate signal;

alternating the phases of said first delay line and said second delay line, concurrently launching a second input signal into said second delay line and applying a reset signal to said first delay line, such that all signals propagating through said first delay line are eliminated;

initiating an evaluate signal;

receiving a second output signal from said second delay line in response to said second input signal;

receiving said evaluate signal; and

asserting an output logic signal dependent on the time of said receiving said second output signal relative to the time of said receiving said evaluate signal.

7. The method of claim 6 wherein said output logic signal is selected from the group consisting of high slow, low slow, high fast, and low fast.

8. The method of claim 6 further comprising fabricating said circuit, said first delay line, and said second delay line on a common semiconductor wafer substrate.

9. The method of claim 6 wherein said reset signal is applied by turning on a pull-down nfet, such that a node of one of said first delay line and said second delay line is forced to zero.

10. The method of claim 6 wherein said first and said second input signals, said first and said second reset signals, and said evaluate signal are all timed by timing circuitry.

11. A system for evaluating the speed of a circuit, said system comprising:

means for concurrently launching an input signal into a first delay line and means for applying a reset signal to a second delay line, such that all signals propagating through said second delay line are eliminated;

means for initiating an evaluate signal;

means for receiving an output signal from said first delay line in response to said input signal;

means for receiving said evaluate signal;

means for asserting an output logic signal dependent on the time of said receiving said output signal relative to the time of said receiving said evaluate signal;

means for alternating the phases of said first delay line and said second delay line, such that the functions of said first delay line and said second delay line are interchanged.

12. The system of claim 11 wherein said output logic signal is selected from the group consisting of high slow, low slow, high fast, and low fast.

13. The system of claim 11 further comprising means for applying said reset signal by turning on a pull-down nfet, such that a node of one of said first delay line and said second delay line is forced to zero.

14. The system of claim 11 wherein said means for launching said input signal, means for applying said reset signal, and means for initiating an evaluate signal comprise timing signals.

15. A method for evaluating the speed of a circuit, said method comprising:

determining during a first operational phase of a first operational cycle the propagation speed of a first signal in a first signal propagation path, and concurrently preventing all signals from propagating in a second signal propagation path substantially parallel with said first signal propagation path; and

determining during a second operational phase alternating with said first operational phase the propagation speed of a second signal in said second signal propagation path, and concurrently preventing all signals from propagating in said first signal propagation path.

16. The method of claim 15 wherein said propagation speed is determined by comparing the propagation time of an evaluate signal relative to the propagation time of one of said respective first signal and said second signal.

17. The method of claim 15 further comprising asserting an output logic signal dependent on said propagation time of one of said respective first signal and said second signal relative to said propagation time of said evaluate signal.

18. The method of claim 17 wherein said output logic signal is selected from the group consisting of high slow, low slow, high fast, and low fast.

19. The method of claim 15 wherein said preventing all signals from propagating comprises applying a reset signal.

20. The method of claim 19 wherein said first signal propagation path and said second signal propagation path comprise respectively a first delay line and a second delay line.

21. The method of claim 20 wherein said reset signal is applied using a pull-down nfet, such that a node of one of said first delay line and said second delay line is forced to zero.

22. The method of claim 20 further comprising fabricating said circuit, said first delay line, and said second delay line on a common semiconductor wafer substrate.

23. The method of claim 16 wherein said first and said second input signals, said preventing, and said evaluate signal are all timed by timing circuitry.